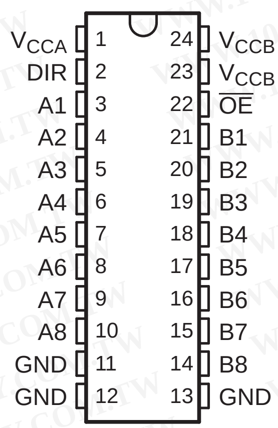
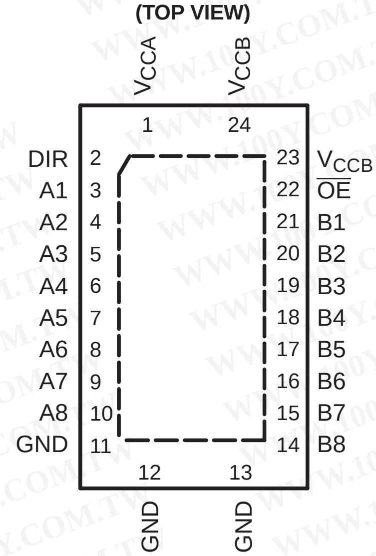
FEATURES

- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All I/O Ports Are in the High-Impedance State
- I_{off} Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- Max Data Rates:
  - 320 Mbps ($V_{CCA} \geq 1.8$ V and $V_{CCB} \geq 1.8$ V)
  - 170 Mbps ($V_{CCA} \leq 1.8$ V or $V_{CCB} \leq 1.8$ V)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGV OR PW PACKAGE
(TOP VIEW)



RHL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 8-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVCH8T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RHL	Reel of 1000	SN74AVCH8T245RHLR	WP245
	TSSOP – PW	Tube of 60	SN74AVCH8T245PW	WP245
		Reel of 2000	SN74AVCH8T245PWR	
	TVSOP – DGV	Reel of 2000	SN74AVCH8T245DGVR	WP245

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74AVCH8T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCH8T245 is designed so the control pins (DIR and $\overline{OE}$) are supplied by V_{CCA}.

The SN74AVCH8T245 solution is compatible with a single-supply system and can be replaced later with a '245 function, with minimal printed circuit board redesign.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

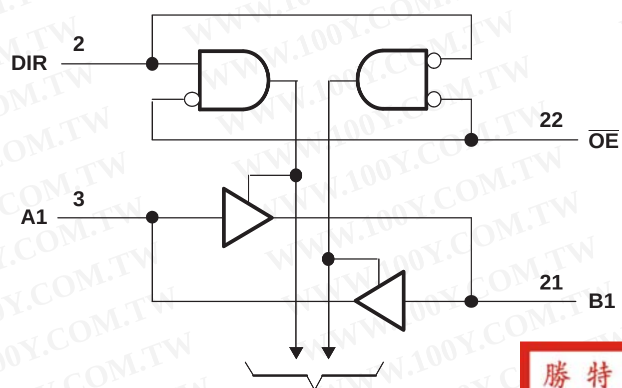
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All output Hi-Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[2][3]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DGV package		86	°C/W
		PW package		88	
		RHL package		43	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)(2)(3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.2 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V		$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V			$V_{CCA} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C MIN	TYP	MAX	–40°C to 85°C MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 μA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V
	I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
	I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
	I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
	I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
	I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}	I_{OL} = 100 μA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
	I_{OL} = 3 mA		1.2 V	1.2 V		0.15				
	I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
	I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
	I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
	I_{OL} = 12 mA		3 V	3 V					0.7	
I_I Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μA
I_{BHL} (3)	V_I = 0.42 V		1.2 V	1.2 V		25				μA
	V_I = 0.49 V		1.4 V	1.4 V				15		
	V_I = 0.58 V		1.65 V	1.65 V				25		
	V_I = 0.7 V		2.3 V	2.3 V				45		
	V_I = 0.8 V		3.3 V	3.3 V				100		
I_{BHH} (4)	V_I = 0.78 V		1.2 V	1.2 V		–25				μA
	V_I = 0.91 V		1.4 V	1.4 V				–15		
	V_I = 1.07 V		1.65 V	1.65 V				–25		
	V_I = 1.6 V		2.3 V	2.3 V				–45		
	V_I = 2 V		3.3 V	3.3 V				–100		
I_{BHLO} (5)	V_I = 0 to V_{CC}		1.2 V	1.2 V		50				μA
			1.6 V	1.6 V				125		
			1.95 V	1.95 V				200		
			2.7 V	2.7 V				300		
			3.6 V	3.6 V				500		
I_{BHHO} (6)	V_I = 0 to V_{CC}		1.2 V	1.2 V		–50				μA
			1.6 V	1.6 V				–125		
			1.95 V	1.95 V				–200		
			2.7 V	2.7 V				–300		
			3.6 V	3.6 V				–500		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Electrical Characteristics (continued)[1][2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 V to 3.6 V		±0.1	±1		±5	µA
	B port		0 V to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}[3]	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$	3.6 V	3.6 V		±0.5	±2.5		±5	µA
	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE}$ = don't care	0 V	3.6 V					±5	
	A port		3.6 V	0 V					±5	
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					8	µA
			0 V	3.6 V					–2	
			3.6 V	0 V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					8	µA
			0 V	3.6 V					8	
			3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V					16	µA
C_i	Control inputs	V_I = 3.3 V or GND	3.3 V	3.3 V		3.5			4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND	3.3 V	3.3 V		6			7	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.1	2.6	2.5	3	3.5	ns
t_{PHL}			3.1	2.6	2.5	3	3.5	
t_{PLH}	B	A	3.1	2.7	2.5	2.4	2.3	ns
t_{PHL}			3.1	2.7	2.5	2.4	2.3	
t_{PZH}	$\overline{OE}$	A	5.3	5.3	5.3	5.3	5.3	ns
t_{PZL}			5.3	5.3	5.3	5.3	5.3	
t_{PZH}	$\overline{OE}$	B	5.1	4	3.5	3.2	3.1	ns
t_{PZL}			5.1	4	3.5	3.2	3.1	
t_{PHZ}	$\overline{OE}$	A	4.8	4.8	4.8	4.8	4.8	ns
t_{PLZ}			4.8	4.8	4.8	4.8	4.8	
t_{PHZ}	$\overline{OE}$	B	4.7	4	4.1	4.3	5.1	ns
t_{PLZ}			4.7	4	4.1	4.3	5.1	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.5	5.4	0.5	4.6	0.5	4.9	0.5	6.8	ns
t_{PHL}			2.7	0.5	5.4	0.5	4.6	0.5	4.9	0.5	6.8	
t_{PLH}	B	A	2.6	0.5	5.4	0.5	5.1	0.5	4.7	0.5	4.5	ns
t_{PHL}			2.6	0.5	5.4	0.5	5.1	0.5	4.7	0.5	4.5	
t_{PZH}	$\overline{OE}$	A	3.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	ns
t_{PZL}			3.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	
t_{PZH}	$\overline{OE}$	B	4.8	1.1	7.6	1.1	7.1	1	5.6	1	5.2	ns
t_{PZL}			4.8	1.1	7.6	1.1	7.1	1	5.6	1	5.2	
t_{PHZ}	$\overline{OE}$	A	3.1	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	ns
t_{PLZ}			3.1	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	
t_{PHZ}	$\overline{OE}$	B	4.1	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	ns
t_{PLZ}			4.1	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.5	5.1	0.5	4.4	0.5	4	0.5	3.9	ns
t_{PHL}			2.5	0.5	5.1	0.5	4.4	0.5	4	0.5	3.9	
t_{PLH}	B	A	2.5	0.5	4.6	0.5	4.4	0.5	3.9	0.5	3.7	ns
t_{PHL}			2.5	0.5	4.6	0.5	4.4	0.5	3.9	0.5	3.7	
t_{PZH}	$\overline{OE}$	A	3	1	6.8	1	6.8	1	6.8	1	6.8	ns
t_{PZL}			3	1	6.8	1	6.8	1	6.8	1	6.8	
t_{PZH}	$\overline{OE}$	B	4.6	1.1	8.2	1	6.7	0.5	5.1	0.5	4.5	ns
t_{PZL}			4.6	1.1	8.2	1	6.7	0.5	5.1	0.5	4.5	
t_{PHZ}	$\overline{OE}$	A	2.8	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	ns
t_{PLZ}			2.8	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	
t_{PHZ}	$\overline{OE}$	B	3.9	0.5	7.8	0.5	6.9	0.5	6	0.5	5.8	ns
t_{PLZ}			3.9	0.5	7.8	0.5	6.9	0.5	6	0.5	5.8	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.4	0.5	4.7	0.5	3.9	0.5	3.1	0.5	2.8	ns
t_{PHL}			2.4	0.5	4.7	0.5	3.9	0.5	3.1	0.5	2.8	
t_{PLH}	B	A	3	0.5	4.9	0.5	4	0.5	3.1	0.5	2.9	ns
t_{PHL}			3	0.5	4.9	0.5	4	0.5	3.1	0.5	2.9	
t_{PZH}	$\overline{OE}$	A	2.2	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	ns
t_{PZL}			2.2	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	
t_{PZH}	$\overline{OE}$	B	4.5	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4	ns
t_{PZL}			4.5	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4	
t_{PHZ}	$\overline{OE}$	A	1.8	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	ns
t_{PLZ}			1.8	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	
t_{PHZ}	$\overline{OE}$	B	3.6	0.5	7.1	0.5	6.3	0.5	5.1	0.5	3.9	ns
t_{PLZ}			3.6	0.5	7.1	0.5	6.3	0.5	5.1	0.5	3.9	

Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	0.5	4.5	0.5	3.7	0.5	2.9	0.5	2.5	ns
t_{PHL}			2.3	0.5	4.5	0.5	3.3	0.5	2.9	0.5	2.5	
t_{PLH}	B	A	3.5	0.5	6.8	0.5	3.9	0.5	2.8	0.5	2.5	ns
t_{PHL}			3.5	0.5	6.8	0.5	3.9	0.5	2.8	0.5	2.5	
t_{PZH}	$\overline{OE}$	A	2	0.5	4	0.5	4	0.5	4	0.5	4	ns
t_{PZL}			2	0.5	4	0.5	4	0.5	4	0.5	4	
t_{PZH}	$\overline{OE}$	B	4.5	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	ns
t_{PZL}			4.5	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	
t_{PHZ}	$\overline{OE}$	A	1.7	0.5	4	0.5	4	0.5	4	0.5	4	ns
t_{PLZ}			1.7	0.5	4	0.5	4	0.5	4	0.5	4	
t_{PHZ}	$\overline{OE}$	B	3.4	0.5	6.9	0.5	6	0.5	4.8	0.5	4.2	ns
t_{PLZ}			3.4	0.5	6.9	0.5	6	0.5	4.8	0.5	4.2	

Operating Characteristics

$T_A = 25°C$

PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2\ V$ TYP	$V_{CCA} = V_{CCB} = 1.5\ V$ TYP	$V_{CCA} = V_{CCB} = 1.8\ V$ TYP	$V_{CCA} = V_{CCB} = 2.5\ V$ TYP	$V_{CCA} = V_{CCB} = 3.3\ V$ TYP	UNIT
C_{pdA} [1]	A to B	Outputs enabled	$C_L = 0$, f = 10 MHz, $t_r = t_f = 1$ ns	1	1	1	1	1	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		12	12	12	13	14	
		Outputs disabled		1	1	1	1	1	
C_{pdB} [1]	A to B	Outputs enabled	$C_L = 0$, f = 10 MHz, $t_r = t_f = 1$ ns	12	12	12	13	14	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	1	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver

Table 1. Typical Total Static Power Consumption ($I_{CCA} + I_{CCB}$)

V_{CCB}	V_{CCA} 0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	UNIT
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	µA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

TYPICAL CHARACTERISTICS

Typical Propagation Delay (A to B) vs Load Capacitance
$T_A = 25°C$, $V_{CCA} = 1.2$ V

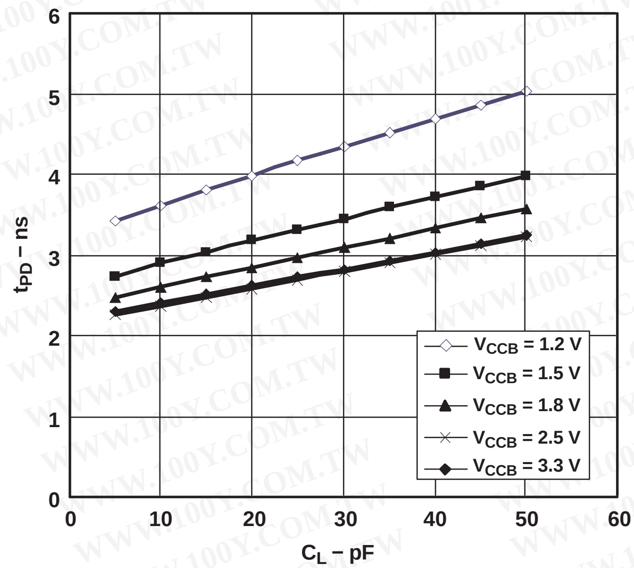


Figure 1.

Typical Propagation Delay (A to B) vs Load Capacitance
$T_A = 25°C$, $V_{CCA} = 1.5$ V

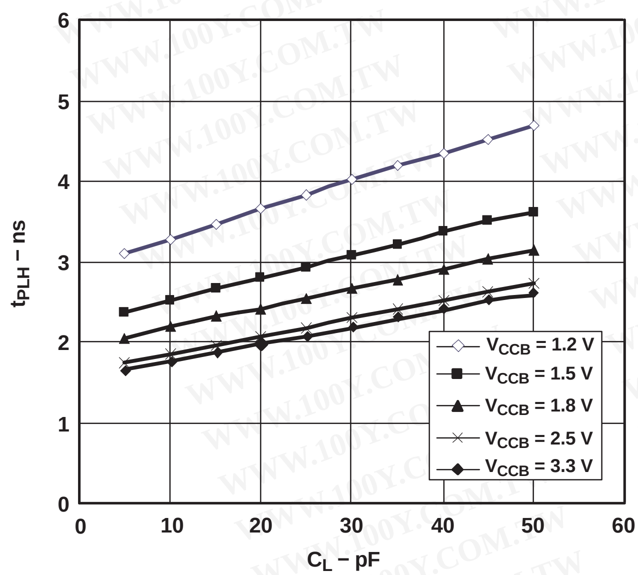


Figure 2.

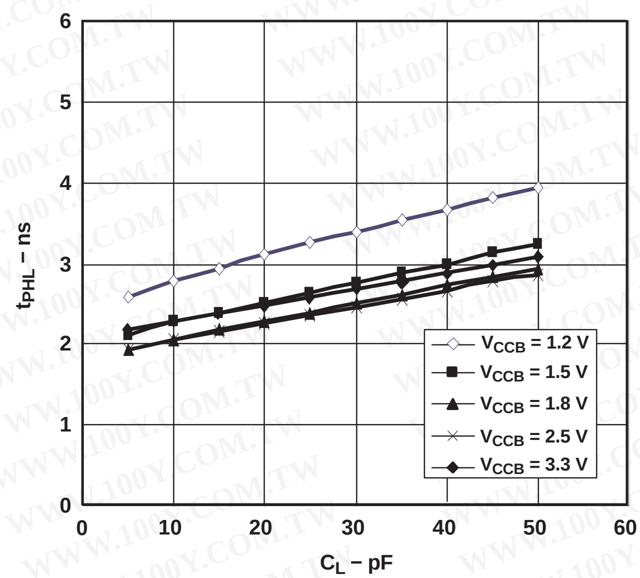


Figure 3.

TYPICAL CHARACTERISTICS (continued)

Typical Propagation Delay (A to B) vs Load Capacitance
$T_A = 25°C, V_{CCA} = 1.8\ V$

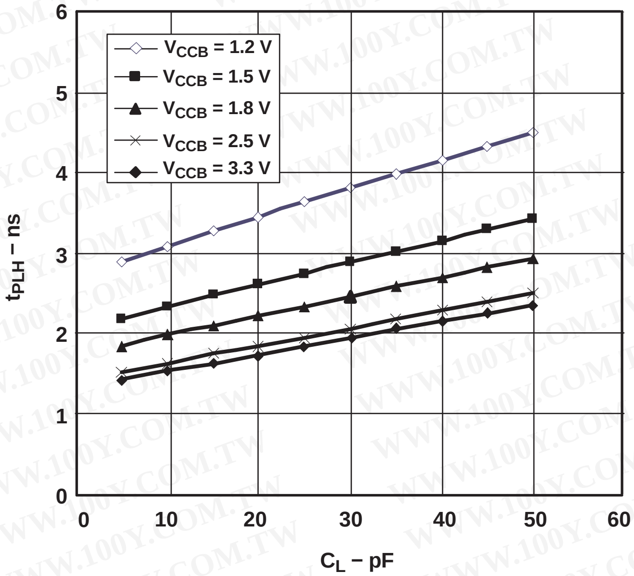


Figure 4.

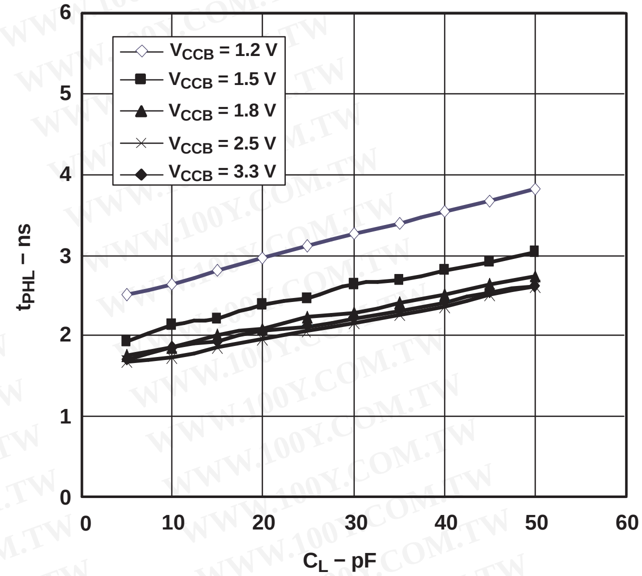


Figure 5.

Typical Propagation Delay (A to B) vs Load Capacitance
$T_A = 25°C, V_{CCA} = 2.5\ V$

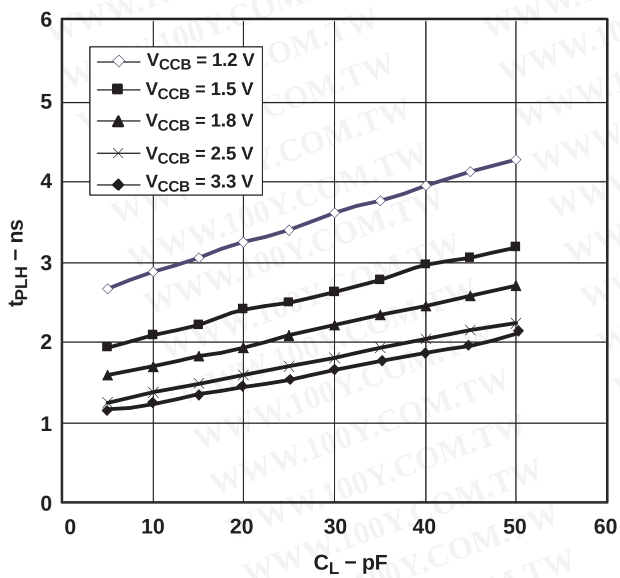


Figure 6.

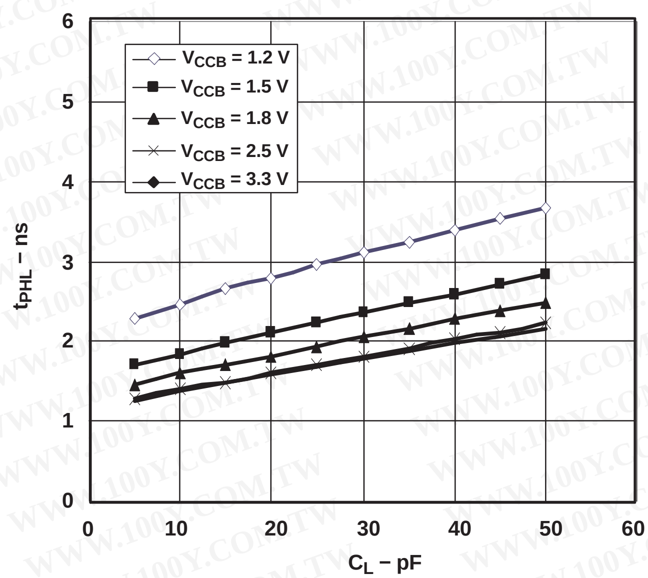


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Typical Propagation Delay (A to B) vs Load Capacitance
$T_A = 25°C$, $V_{CCA} = 3.3$ V

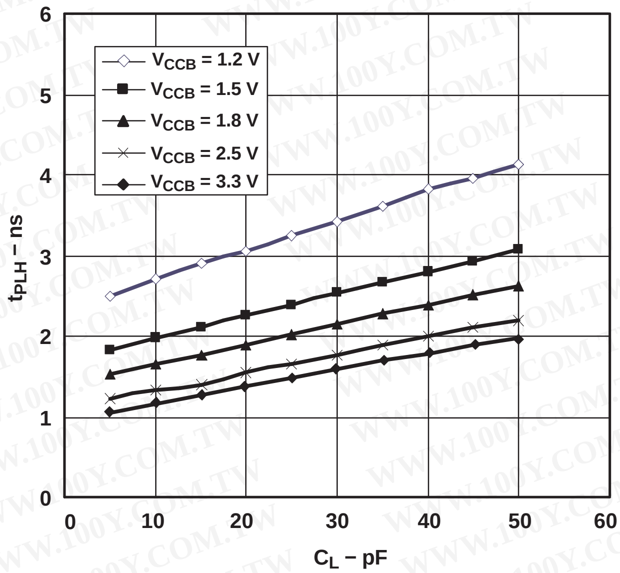


Figure 8.

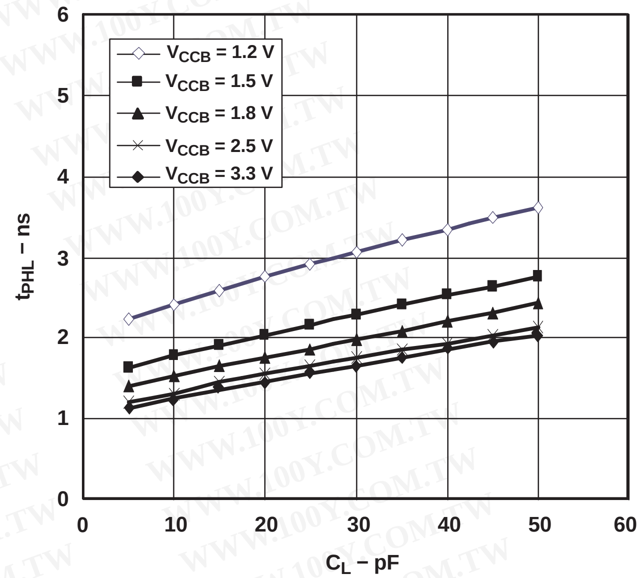
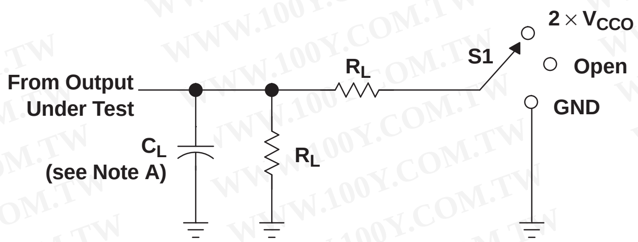


Figure 9.

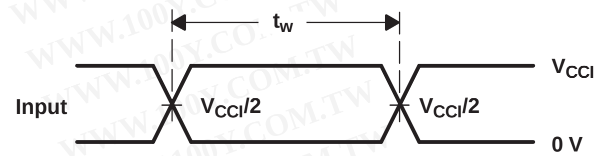
PARAMETER MEASUREMENT INFORMATION



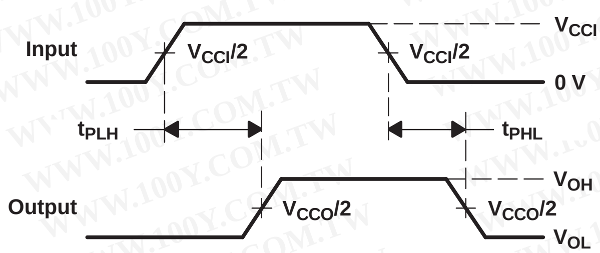
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

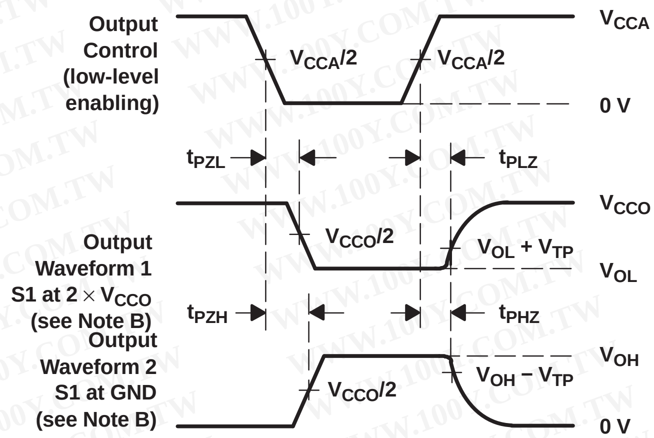
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 10. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVCH8T245DGVRE4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		Samples
74AVCH8T245DGVRG4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		Samples
74AVCH8T245PWRE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
74AVCH8T245PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
74AVCH8T245RHLRG4	ACTIVE	VQFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WP245	Samples
SN74AVCH8T245DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WP245	Samples
SN74AVCH8T245RHLR	ACTIVE	VQFN	RHL	24	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WP245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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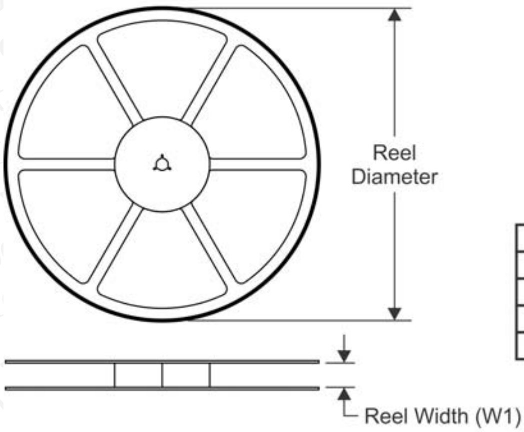
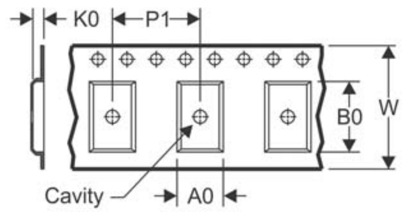
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

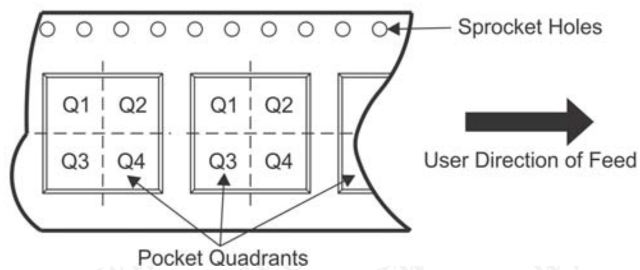
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

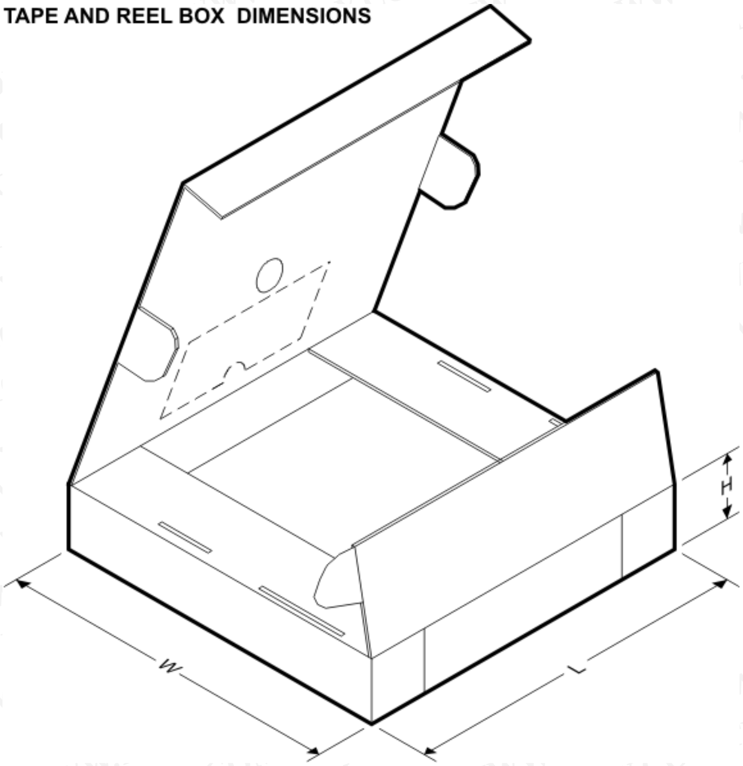
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74AVCH8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

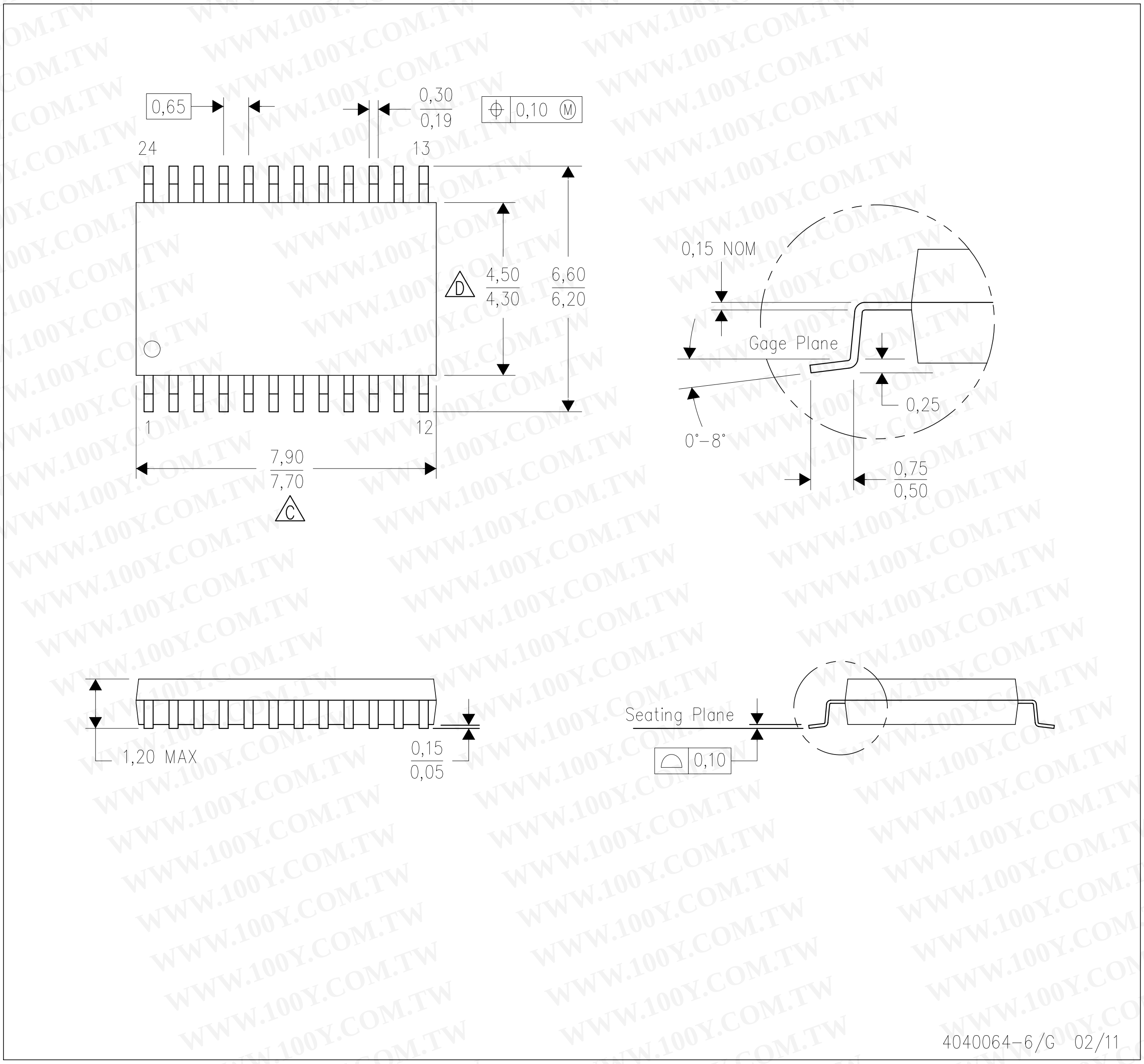
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

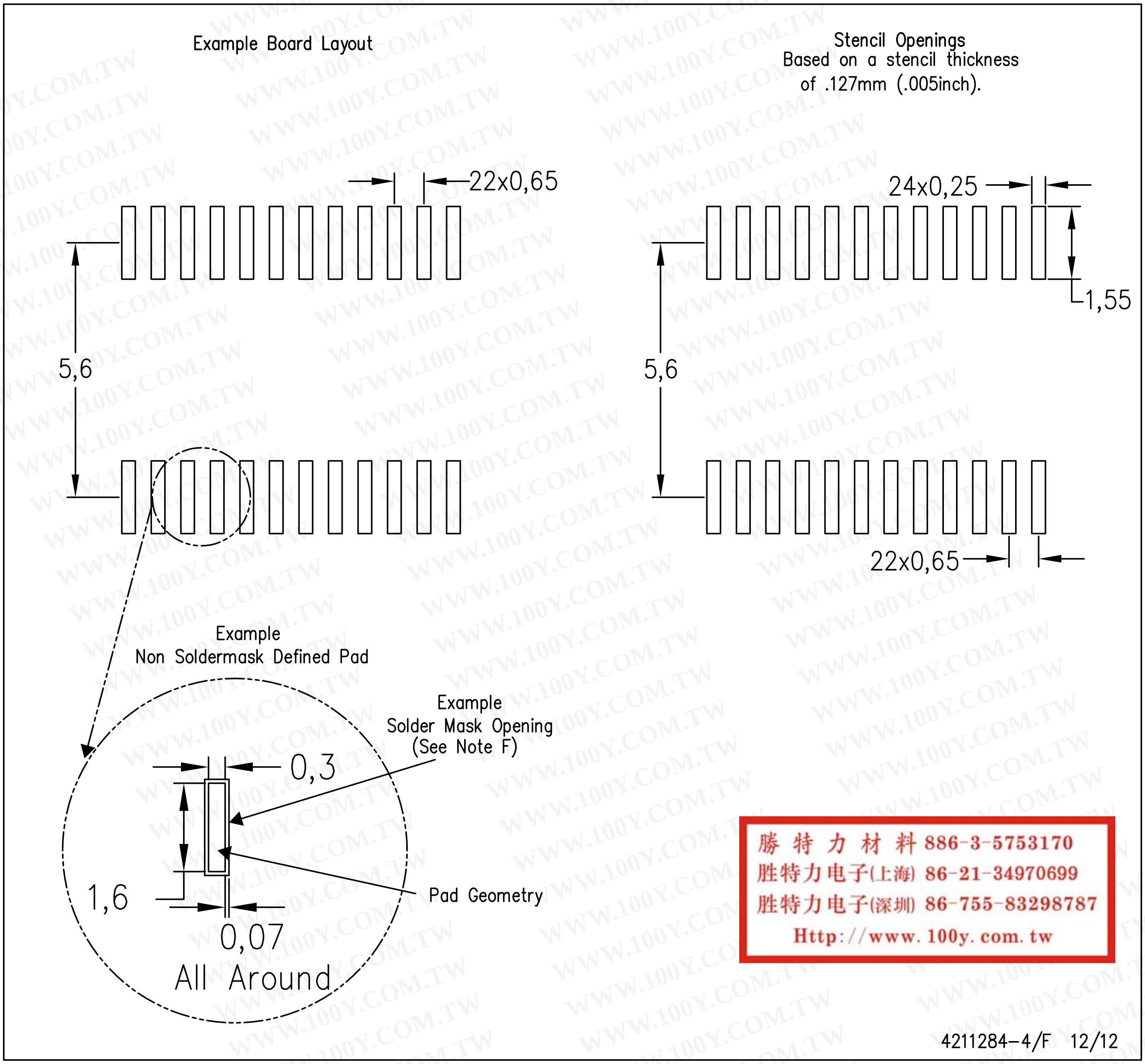
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH8T245DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74AVCH8T245PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74AVCH8T245RHLR	VQFN	RHL	24	1000	210.0	185.0	35.0

PW (R-PDSO-G24) PLASTIC SMALL OUTLINE



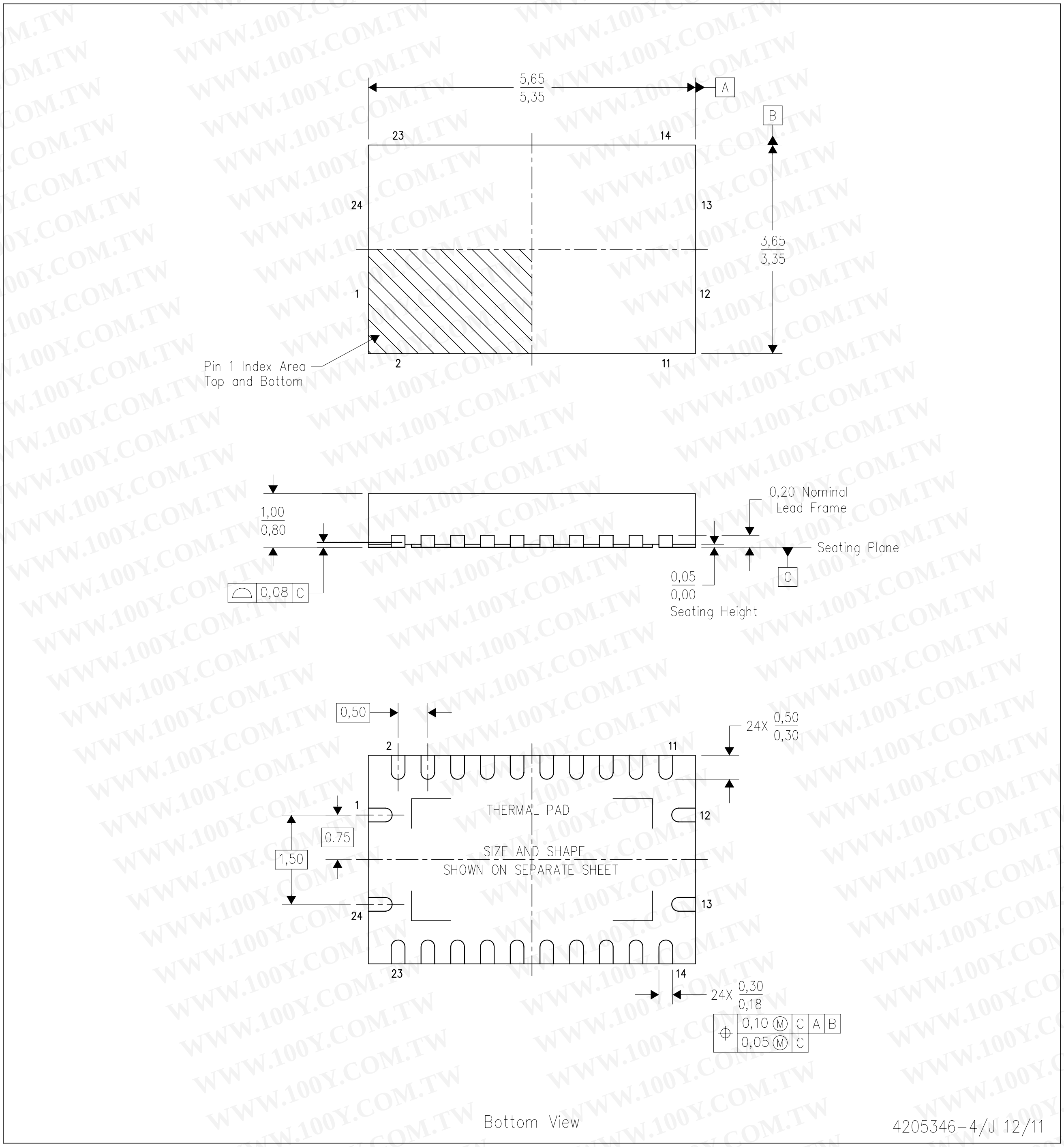
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHL (R-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. JEDEC MO-241 package registration pending.

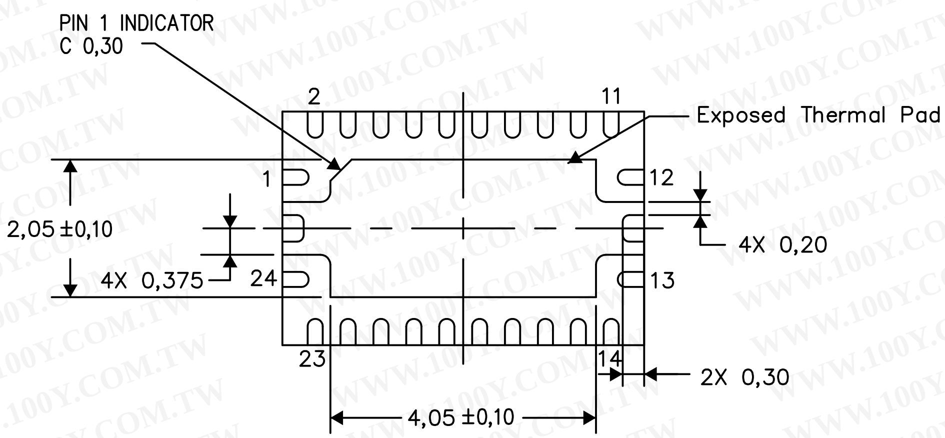
RHL (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



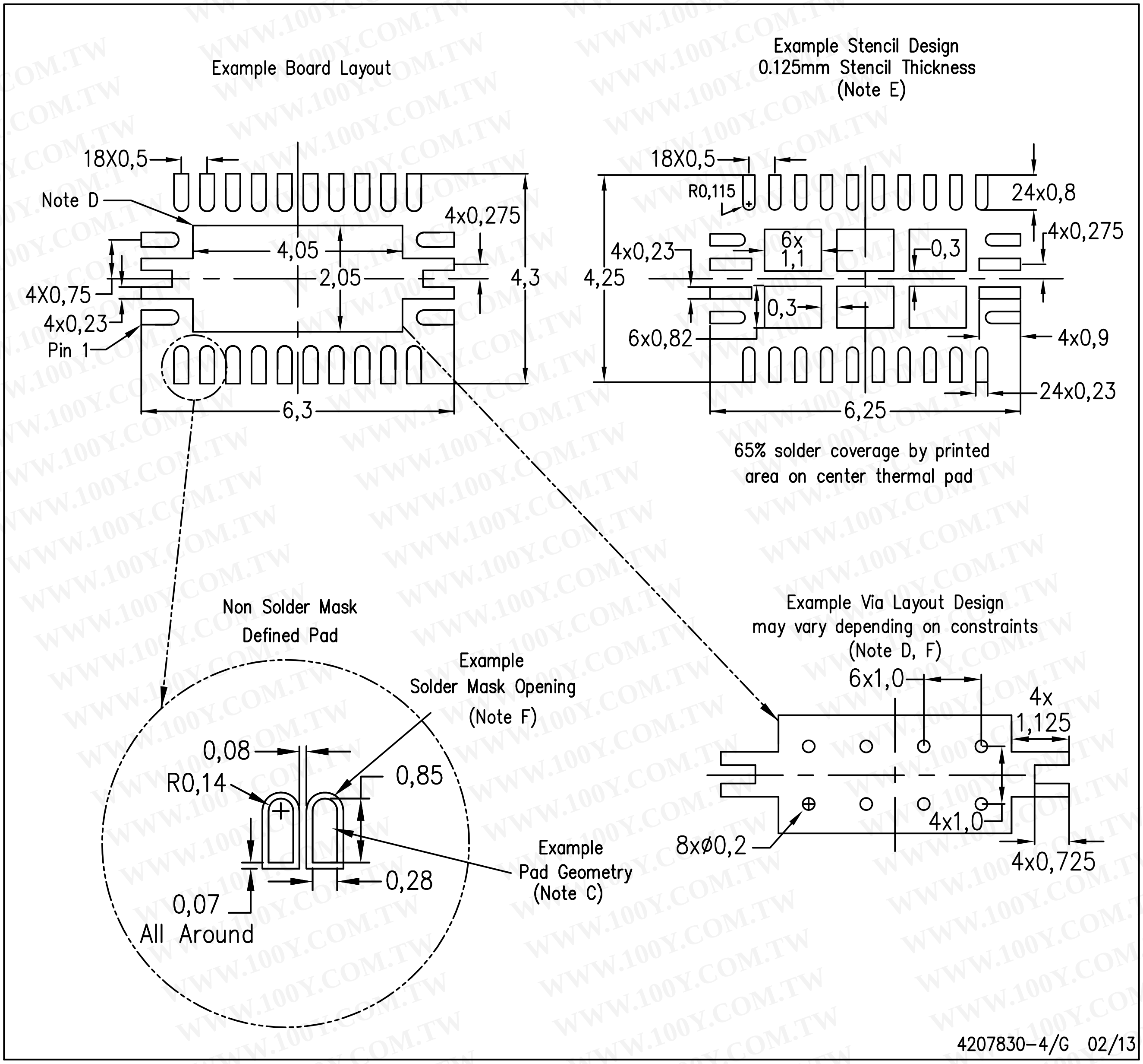
Bottom View

Exposed Thermal Pad Dimensions

4206363-4/M 08/12

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.